SLLS165A – JANUARY 1994 – REVISED JUNE 1994

- Integrated Asynchronous Communications Element
- Consists of Four Improved TL16C550 ACEs Plus Steering Logic
- In FIFO Mode, Each ACE Transmitter and Receiver Is Buffered With 16-Byte FIFO to Reduce the Number of Interrupts to CPU
- In TL16C450 Mode, Hold and Shift Registers Eliminate Need for Precise Synchronization Between the CPU and Serial Data
- Up to 16-MHz Clock Rate for up to 1-Mbaud Operation
- Programmable Baud-Rate Generators Allow Division of Any Input Reference Clock by 1 to ($2^{16}-1$) and Generates Internal 16 × Clock
- Adds or Deletes Standard Asynchronous Communication Bits (Start, Stop, and Parity) to or From the Serial Data Stream
- Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts
- Fully Programmable Serial Interface Characteristics:
  - 5-, 6-, 7-, or 8-Bit Characters
  - Even-, Odd-, or No-Parity Bit
  - 1-, 1 1/2-, or 2-Stop Bit Generation
  - Baud Generation (DC to 256 Kilobits Per Second)
- False-Start Bit Detection
- Complete Status Reporting Capabilities
- Line-Break Generation and Detection
- Internal Diagnostic Capabilities:
  - Loopback Controls for Communications Link Fault Isolation
  - Break, Parity, Overrun, Framing Error Simulation
- Fully Prioritized Interrupt System Controls
- Modem Control Functions ($\overline{\text{CTS}}$, $\overline{\text{RTS}}$, $\overline{\text{DSR}}$, $\overline{\text{DTR}}$, $\overline{\text{RI}}$, and $\overline{\text{DCD}}$)
- 3-State Outputs Provide TTL-Drive Capabilities for Bidirectional Data Bus and Control Bus

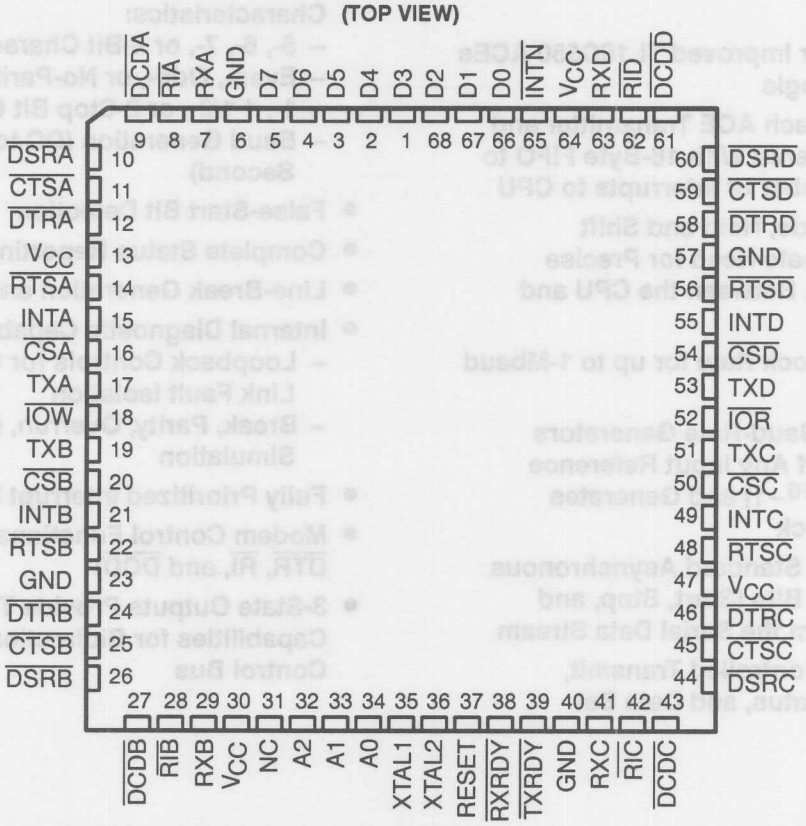
description

The TL16C554 is an enhanced quad version of the TL16C550B asynchronous communications element (ACE). Each channel performs serial-to-parallel conversion on data characters received from peripheral devices or modems and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of each channel of the quad ACE can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the operation performed and any error conditions encountered.

The TL16C554 quad ACE can be placed in an alternate FIFO mode, which activates the internal FIFOs to allow 16 bytes (plus 3 bits of error data per byte in the receiver FIFO) to be stored in both receive and transmit modes. To minimize system overhead and maximize system efficiency, all logic is on the chip. Two pin functions have been provided to allow signalling of DMA transfers. Each ACE includes a programmable, baud-rate generator that can divide the timing reference clock input by a divisor between 1 and ($2^{16}-1$).

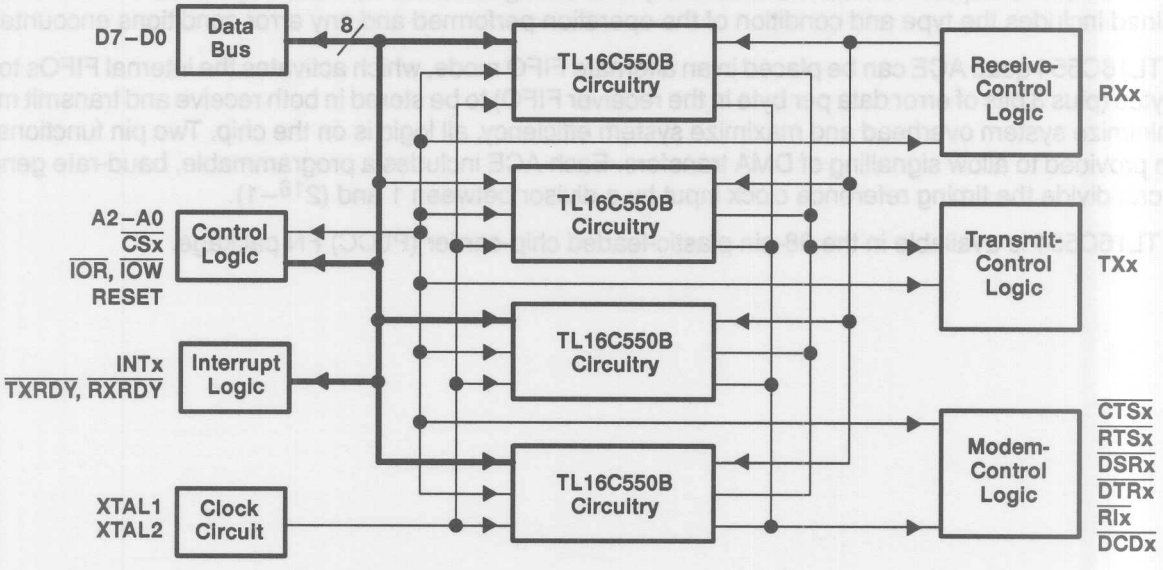
The TL16C554 is available in the 68-pin plastic-leaded chip-carrier (PLCC) FN package.

FN PACKAGE
(TOP VIEW)



NC – No internal connection

functional block diagram†



† For TL16C550 circuitry, refer to the TL16C550B data sheet.

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Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
A0 A1 A2	34 33 32	I	Register select terminals are three inputs used during read and write operations to select the ACE register to read or write.
$\overline{CSA}$, $\overline{CSB}$, $\overline{CSC}$, $\overline{CSD}$	16, 20, 50, 54	I	Chip select. Each chip select enables read and write operations to its respective channel.
$\overline{CTSA}$, $\overline{CTSB}$, $\overline{CTSC}$, $\overline{CTSD}$	11, 25, 45, 59	I	Clear to send. A modem status signal whose condition can be checked by reading bit 4 (CTS) of the modem-status register. $\overline{CTS}$ has no effect on the transmit or receive operation.
D7–D0	66–68 1–5	I/O	Data bus. Eight data lines with 3-state outputs provide a bidirectional path for data, control and status information between the TL16C554 and the CPU. D0 is the least significant bit (LSB).
$\overline{DCDA}$, $\overline{DCDB}$, $\overline{DCDC}$, $\overline{DCDD}$	9, 27, 43, 61	I	Data carrier detect. A low on this terminal indicates the carrier has been detected by the modem. The condition of this signal can be checked by reading bit 7 of the modem-status register.
$\overline{DSRA}$, $\overline{DSRB}$, $\overline{DSRC}$, $\overline{DSRD}$	10, 26, 44, 60	I	Data set ready. A modem status signal whose condition can be checked by reading bit 5 (DSR) of the modem-status register. $\overline{DSR}$ has no effect on the transmit or receive operation.
$\overline{DTRA}$, $\overline{DTRB}$, $\overline{DTRC}$, $\overline{DTRD}$	12, 24, 46, 58	O	Data terminal ready. These outputs indicate to a modem or data set that the ACE is ready to establish communications. They are placed in the active state by setting the DTR bit of the modem-control register to a high level. $\overline{DTR}$ is placed in the inactive state (high) either as a result of the master reset during loop-mode operation or resetting bit 0 ($\overline{DTR}$) of the modem-control register.
$\overline{INTN}$	65	I	Interrupt normal. $\overline{INTN}$ operates in conjunction with bit 3 of the modem-status register (MCR) and affects operation of the interrupts (INTA, INTB, INTC, and INTD) for the four UARTs per the following table.
GND	6, 23, 40, 57		Signal and power ground
INTA, INTB, INTC, INTD	15, 21, 49, 55	O	External interrupt output. These outputs go high (when enabled by the interrupt register) and inform the CPU that the ACE has an interrupt to be serviced. Four conditions that cause an interrupt to be issued are: a receiver error, receiver data available or time out (FIFO mode only), the transmitter holding register is empty, and an enabled modem status interrupt. The interrupt is disabled when it is serviced or as the result of a master reset.
$\overline{IOR}$	52	I	Read strobe. A low level on this input transfers the contents of the TL16C554 data bus to the external CPU bus.
$\overline{IOW}$	18	I	Write strobe. This input allows the CPU to write into the selected by the address register.
RESET	37	I	Master reset. When active, RESET clears most ACE registers and sets the state of various signals. The transmitter output and the receiver input is disabled during reset time.
$\overline{RIA}$, $\overline{RIB}$, $\overline{RIC}$, $\overline{RID}$	8, 28, 42, 62	I	Ring detect indicator. A low on these inputs indicates the modem has received a ring signal from the telephone line. The condition of this signal can be checked by reading bit 6 of the modem-status register.
$\overline{RTSA}$, $\overline{RTSB}$, $\overline{RTSC}$, $\overline{RTSD}$	14, 22, 48, 56	O	Request to send. When active, these terminals inform the modem or data set that the ACE is ready to receive data. Writing a 1 in the modem-control register sets this bit to a low state. After reset, this terminal is set high. These terminals have no effect on the transmit or receive operation.
RXA, RXB RXC, RXD	7, 29, 41, 63	I	Serial input. Serial data input from a connected communications device. During loopback mode, the RX input is disabled from external connection and connected to the TX output internally.
$\overline{RXRDY}$	38	O	Receive ready. $\overline{RXRDY}$ goes low when the receive FIFO is full. It can be used as a single transfer or multitransfer.
TXA, TXB TXC, TXD	17, 19, 51, 53	O	Transmit outputs. Composite serial data output to a connected communications device. TXA, TXB, TXC, and TXD are set to the marking (logic 1) state as a result of reset.

$\overline{INTN}$	OPERATION OF INTERRUPTS
Brought low or allowed to float	Interrupts are enabled according to the state of OUT2 (MCR bit 3). If MCR bit 3 is low (0), the 3-state interrupt output of that UART is in the high-impedance state. If MCR bit 3 is high (1), the interrupt output of the UART is enabled.
Brought high	Interrupts are always enabled, overriding the OUT2 enables.

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{TXRDY}}$	39	O	Transmit ready. $\overline{\text{TXRDY}}$ goes low when the transmit FIFO is full. It can be used as a single transfer or multitransfer function.
V_{CC}	13, 30, 47, 64		Power supply
XTAL1	35	I	Crystal input 1 or external clock input. A crystal can be connected to this terminal and XTAL2 to utilize the internal-oscillator circuit. An external clock can be connected to drive the internal clock circuits.
XTAL2	36	O	Crystal output 2 or buffered clock output (see XTAL1).

absolute maximum ratings over free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage range at any input, V_I ..... −0.5 V to 7 V
Output voltage range, V_O ..... −0.5 V to V_{CC} + 3 V
Continuous total power dissipation at (or below) 70°C ..... 500 mW
Operating free-air temperature range, T_A ..... −0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage levels are with respect to GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Clock high-level input voltage at XTAL1, $V_{IH(CLK)}$	2		V_{CC}	V
Clock low-level input voltage at XTAL1, $V_{IL(CLK)}$	−0.5		0.8	V
High-level input voltage, V_{IH}	2		V_{CC}	V
Low-level input voltage, V_{IL}	−0.5		0.8	V
Clock frequency, f_{clock}			16	MHz
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}‡	High-level output voltage	I_{OH} = –1 mA	2.4			V
V_{OL}‡	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
I_{lkg}	Input leakage current	V_{CC} = 5.25 V, GND = 0, V_I = 0 to 5.25 V, All other pins floating			±10	µA
I_{OZ}	High-impedance output current	V_{CC} = 5.25 V, GND = 0, V_O = 0 to 5.25 V, Chip selected in write mode or chip deselected			±20	µA
I_{CC}	Supply current	V_{CC} = 5.25 V, T_A = 25°C, RX, $\overline{DSR}$, $\overline{DCD}$, CTS, and $\overline{RI}$ at 2 V, All other inputs at 0.8 V, XTAL1 at 4 MHz, No load on outputs, Baud rate = 50 kilobits per second			50	mA
$C_{i(XTAL1)}$	Clock input capacitance	V_{CC} = 0, V_{SS} = 0, All other pins grounded, f = 1 MHz, T_A = 25°C		15	20	pF
$C_{o(XTAL2)}$	Clock output capacitance			20	30	pF
C_i	Input capacitance			6	10	pF
C_o	Output capacitance			10	20	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ These parameters apply for all outputs except XTAL2.

clock timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 1)

		MIN	MAX	UNIT
t_{w1}	Pulse duration, clock high (external clock)	31		ns
t_{w2}	Pulse duration, clock low (external clock)	31		ns
t_{w3}	Pulse duration, RESET	1000		ns

read-cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 4)

		MIN	MAX	UNIT
t_{w4}	Pulse duration, $\overline{IOR}$ low	75		ns
t_{su1}	Setup time, $\overline{CSx}$ valid before $\overline{IOR}$ low (see Note 2)	10		ns
t_{su2}	Setup time, A2–A0 valid before $\overline{IOR}$ low (see Note 2)	15		ns
t_{h1}	Hold time, A2–A0 valid after $\overline{IOR}$ high (see Note 2)	0		ns
t_{h2}	Hold time, $\overline{CSx}$ valid after $\overline{IOR}$ high (see Note 2)	0		ns
t_{d1}	Delay time, $t_{su2} + t_{w4} + t_{d2}$ (see Note 3)	140		ns
t_{d2}	Delay time, $\overline{IOR}$ high to $\overline{IOR}$ or $\overline{IOW}$ low	50		ns

NOTES: 2. The internal address strobe is always active.
3. In the FIFO mode, t_{d1} = 425 ns (min) between reads of the receiver FIFO and the status registers (IIR and LSR).

write-cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 5)

		MIN	MAX	UNIT
t_{w5}	Pulse duration, $\overline{IOW}\downarrow$	50		ns
t_{su3}	Setup time, $\overline{CSx}$ valid before $\overline{IOW}\downarrow$ (see Note 2)	10		ns
t_{su4}	Setup time, A2–A0 valid before $\overline{IOW}\downarrow$ (see Note 2)	15		ns
t_{su5}	Setup time, D7–D0 valid before $\overline{IOW}\uparrow$	10		ns
t_{h3}	Hold time, A2–A0 valid after $\overline{IOW}\uparrow$ (see Note 2)	5		ns
t_{h4}	Hold time, $\overline{CSx}$ valid after $\overline{IOW}\uparrow$ (see Note 2)	5		ns
t_{h5}	Hold time, D7–D0 valid after $\overline{IOW}\uparrow$	25		ns
t_{d3}	Delay time, $t_{su4} + t_{w5} + t_{d4}$	120		ns
t_{d4}	Delay time, $\overline{IOW}\uparrow$ to $\overline{IOW}$ or $\overline{IOR}\downarrow$	55		ns

NOTE 2: The internal address strobe is always active.

read-cycle switching characteristics over recommended ranges of operating free-air temperature and supply voltage, C_L = 100 pF (see Note 4 and Figure 4)

PARAMETER		MIN	MAX	UNIT
t_{en}	Enable time, $\overline{IOR}\downarrow$ to D7–D0 valid		30	ns
t_{dis}	Disable time, $\overline{IOR}\uparrow$ to D7–D0 released	0	20	ns

NOTE 4: V_{OL} and V_{OH} (and the external loading) determine the charge and discharge time.

transmitter switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figures 6, 7, and 8)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d5}	Delay time, INTx↓ to TXx↓ at start		8	24	RCLK cycles
t_{d6}	Delay time, TXx↓ at start to INTx↑	See Note 5	8	8	RCLK cycles
t_{d7}	Delay time, $\overline{IOW}$ (WR THR) to INTx↑	See Note 5	16	32	RCLK cycles
t_{d8}	Delay time, TXx↓ at start to $\overline{TXRDY}\downarrow$	C_L = 100 pF		8	RCLK cycles
t_{pd1}	Propagation delay time, $\overline{IOW}$ (WR THR)↓ to INTx↓	C_L = 100 pF		35	ns
t_{pd2}	Propagation delay time, $\overline{IOR}$ (RD IIR)↑ to INTx↓	C_L = 100 pF		30	ns
t_{pd3}	Propagation delay time, $\overline{IOW}$ (WR THR)↑ to $\overline{TXRDY}\uparrow$	C_L = 100 pF		50	ns

NOTE 5: If the transmitter interrupt delay is active, this delay is lengthened by one character time minus the last stop bit time.

receiver switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figures 9 through 13)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{d9}	Delay time, stop bit to INTx↑ or stop bit to $\overline{\text{RXRDY}}$↓ or read RBR to set interrupt	See Note 6		1	RCLK cycle
t_{pd4}	Propagation delay time, Read RBR/LSR to INTx↓/LSR interrupt↓	C_L = 100 pF, See Note 7		40	ns
t_{pd5}	Propagation delay time, $\overline{\text{IOR}}$ RCLK↓ to $\overline{\text{RXRDY}}$↑	See Note 7		30	ns

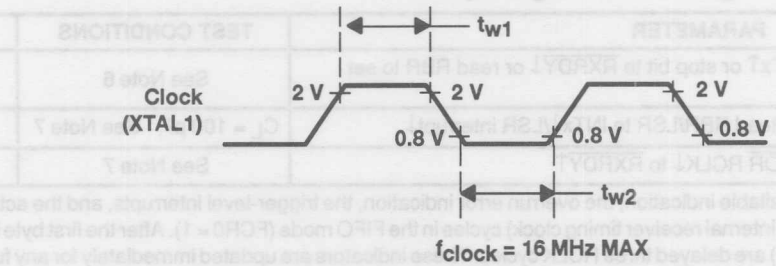
NOTES: 6. The receiver data available indication, the overrun error indication, the trigger-level interrupts, and the active $\overline{\text{RXRDY}}$ indication are delayed three RCLK (internal receiver timing clock) cycles in the FIFO mode (FCR0 = 1). After the first byte has been received, status indicators (PE, FE, BI) are delayed three RCLK cycles. These indicators are updated immediately for any further bytes received after $\overline{\text{IOR}}$ goes active for a read from the RBR register. There are eight RCLK cycle delays for trigger change level interrupts.

7. RCLK is an internal signal derived from DLL and DLM divisor latches.

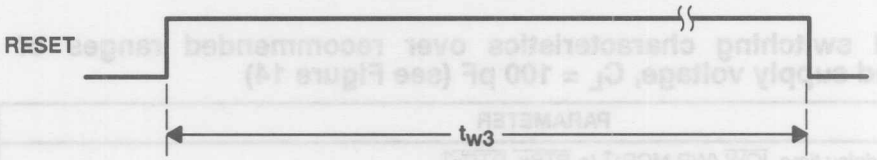
modem-control switching characteristics over recommended ranges of operating free-air temperature and supply voltage, C_L = 100 pF (see Figure 14)

	PARAMETER	MIN	MAX	UNIT
t_{pd6}	Propagation delay time, $\overline{\text{IOW}}$ (WR MCR)↑ to $\overline{\text{RTSx}}$, $\overline{\text{DTRx}}$↑		50	ns
t_{pd7}	Propagation delay time, modem input $\overline{\text{CTSx}}$, $\overline{\text{DSRx}}$, and $\overline{\text{DCDx}}$ ↓↑ to INTx↑		30	ns
t_{pd8}	Propagation delay time, $\overline{\text{IOR}}$ (RD MSR)↑ to interrupt↓		35	ns
t_{pd9}	Propagation delay time, $\overline{\text{RIx}}$↑ to $\overline{\text{INTx}}$↑		30	ns

PARAMETER MEASUREMENT INFORMATION

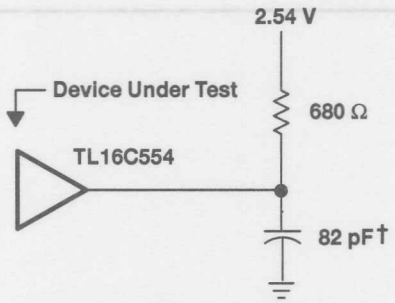


(a) CLOCK INPUT VOLTAGE WAVEFORM



(b) RESET VOLTAGE WAVEFORM

Figure 1. Clock Input and RESET Voltage Waveforms



† Includes scope and jig capacitance

Figure 2. Output Load Circuit

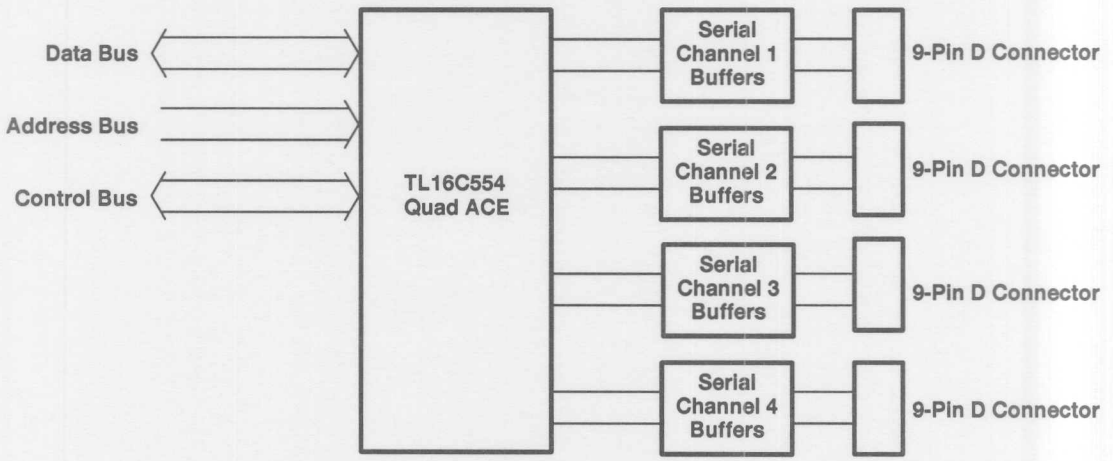


Figure 3. Basic Test Configuration

PARAMETER MEASUREMENT INFORMATION

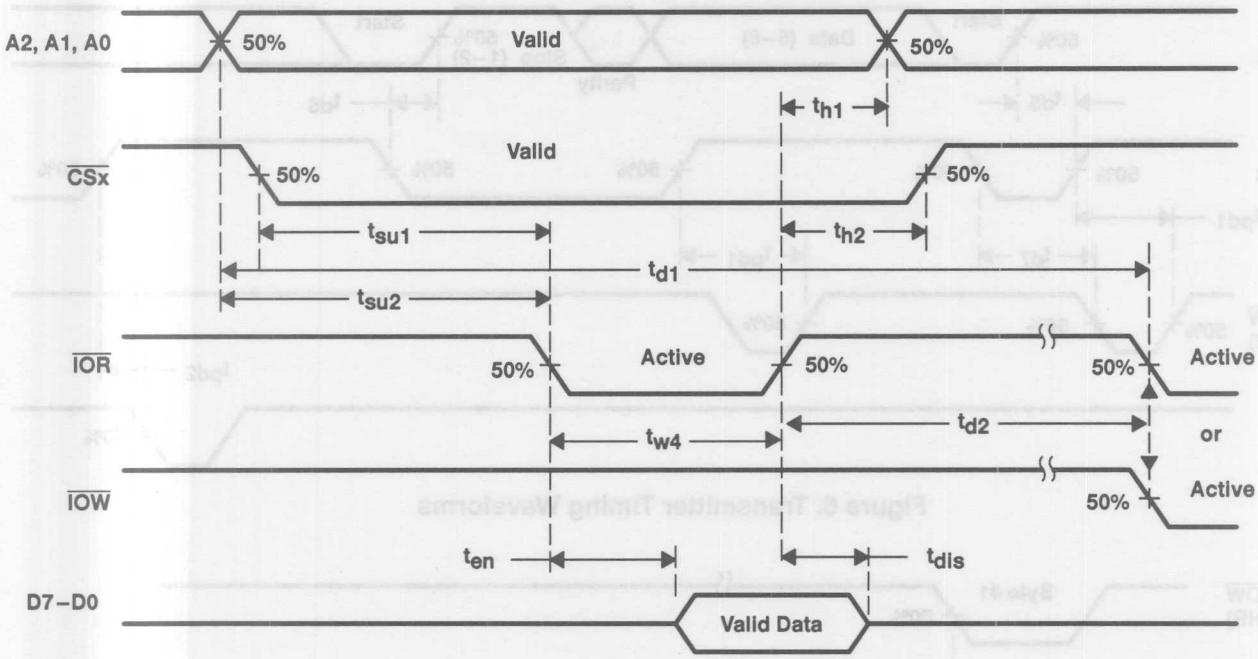


Figure 4. Read-Cycle Timing Waveforms

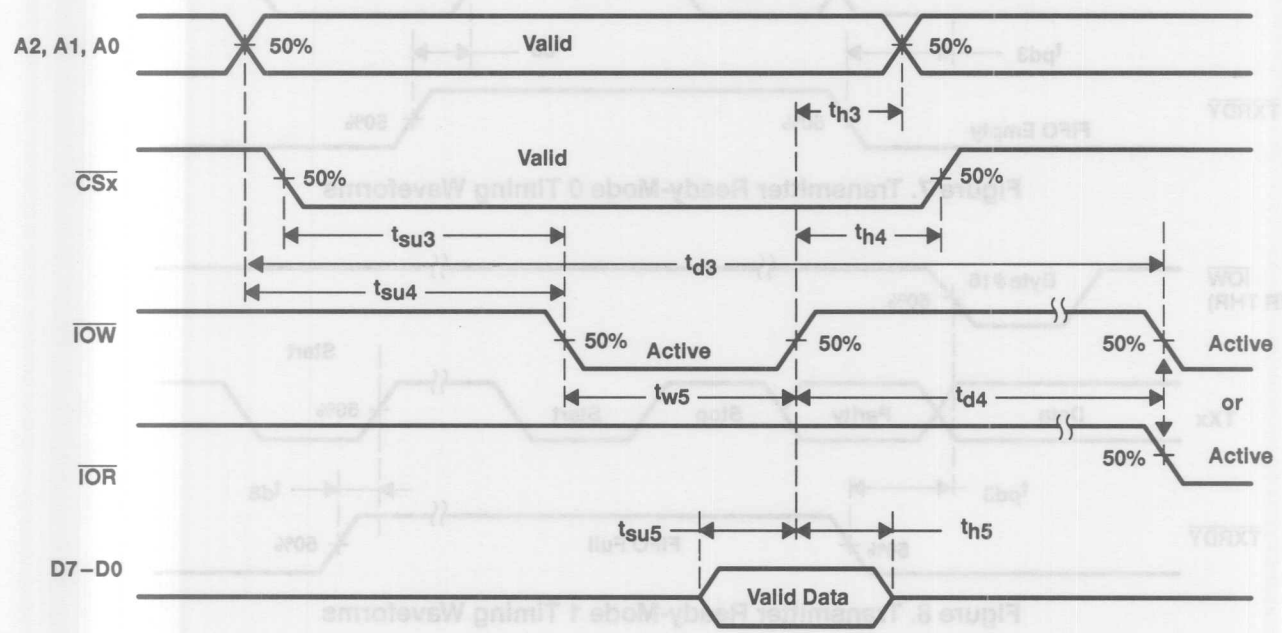


Figure 5. Write-Cycle Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

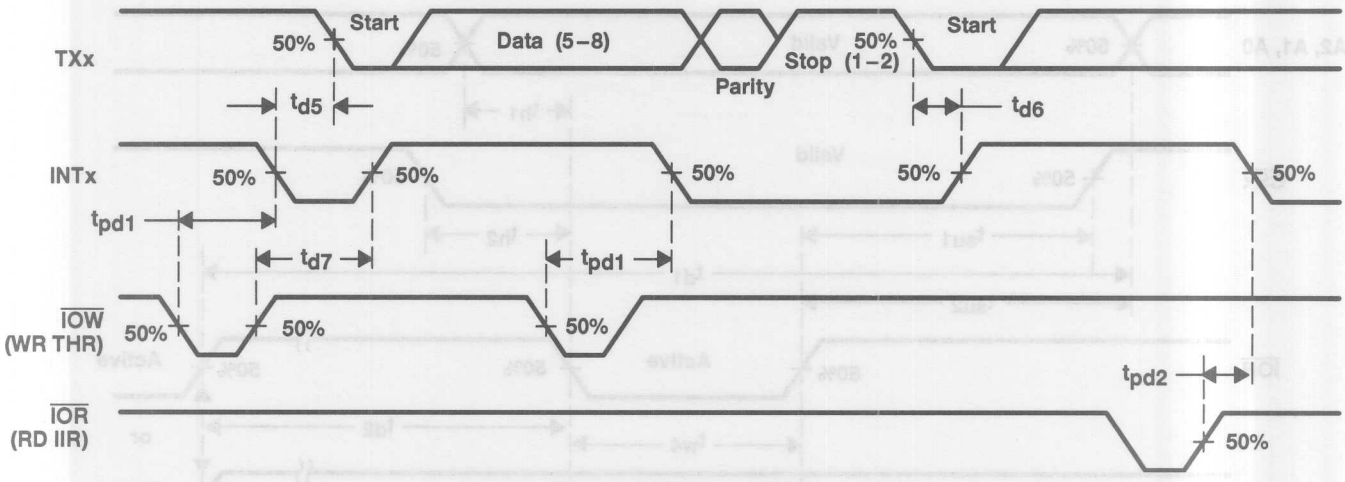


Figure 6. Transmitter Timing Waveforms

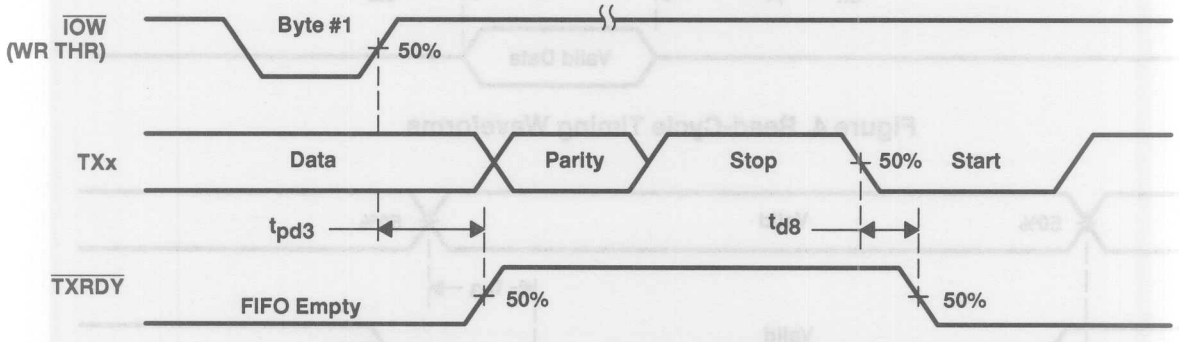


Figure 7. Transmitter Ready-Mode 0 Timing Waveforms

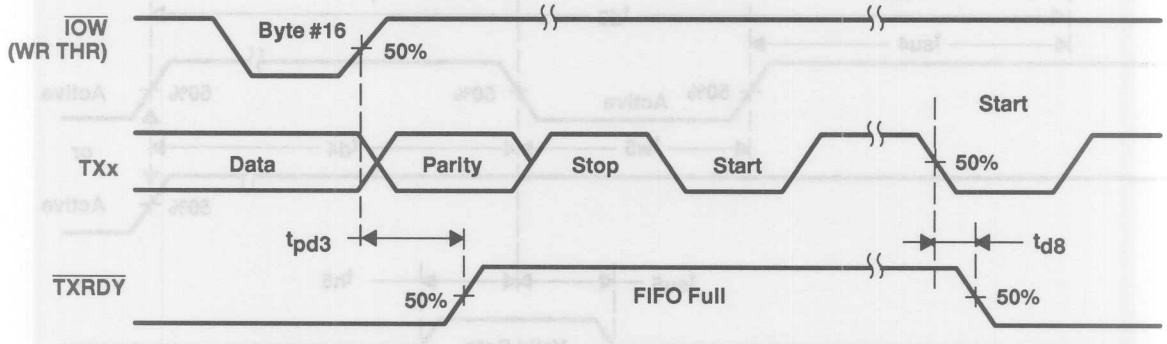


Figure 8. Transmitter Ready-Mode 1 Timing Waveforms

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PARAMETER MEASUREMENT INFORMATION

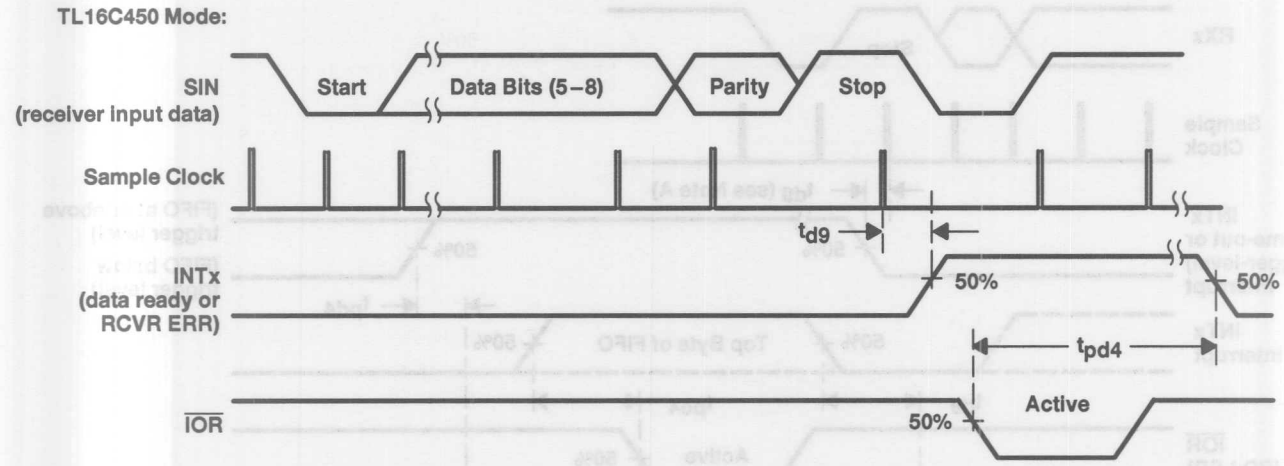


Figure 9. Receiver Timing

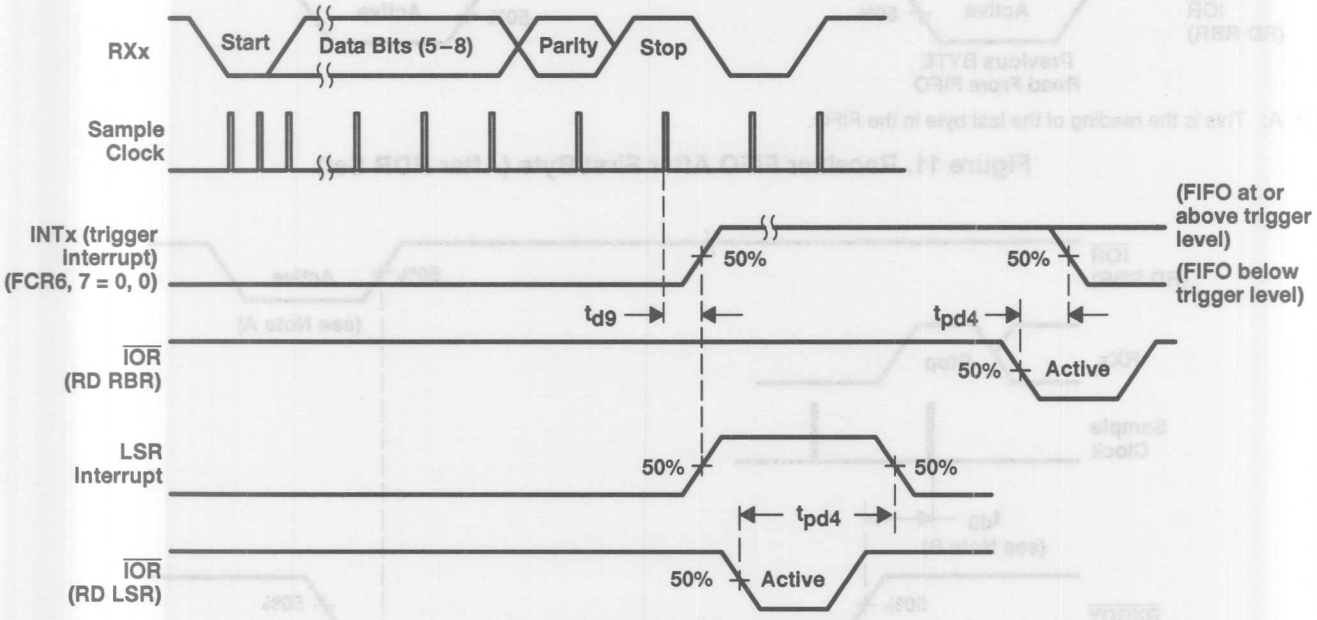
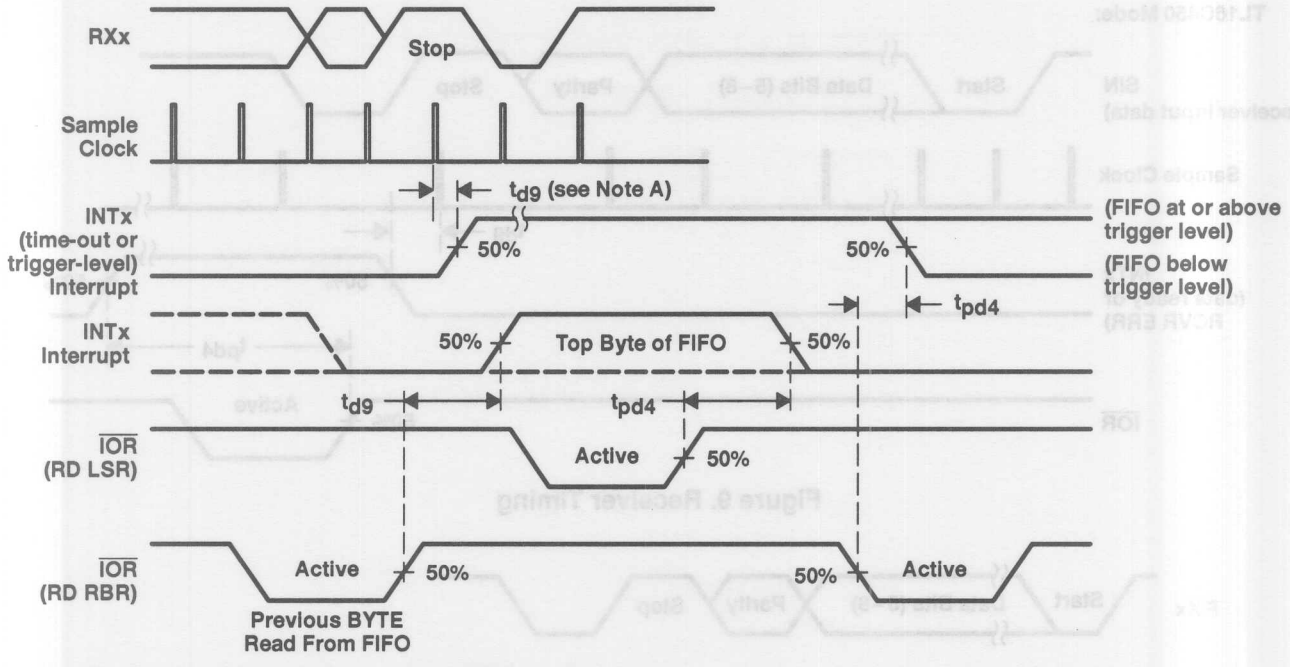


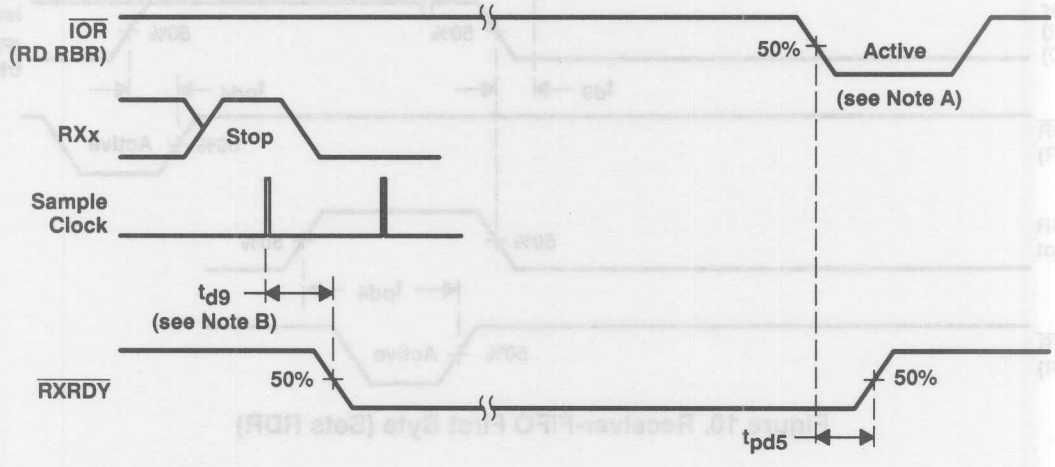
Figure 10. Receiver-FIFO First Byte (Sets RDR)

PARAMETER MEASUREMENT INFORMATION



NOTE A: This is the reading of the last byte in the FIFO.

Figure 11. Receiver FIFO After First Byte (After RDR Set)



NOTES: A. This is the reading of the last byte in the FIFO.
B. If FCR0 = 1, then t_{d9} = 3 RCLK cycles. For a time-out interrupt, t_{d9} = 8 RCLK cycles.

Figure 12. Receiver Ready-Mode 0 Timing Waveforms

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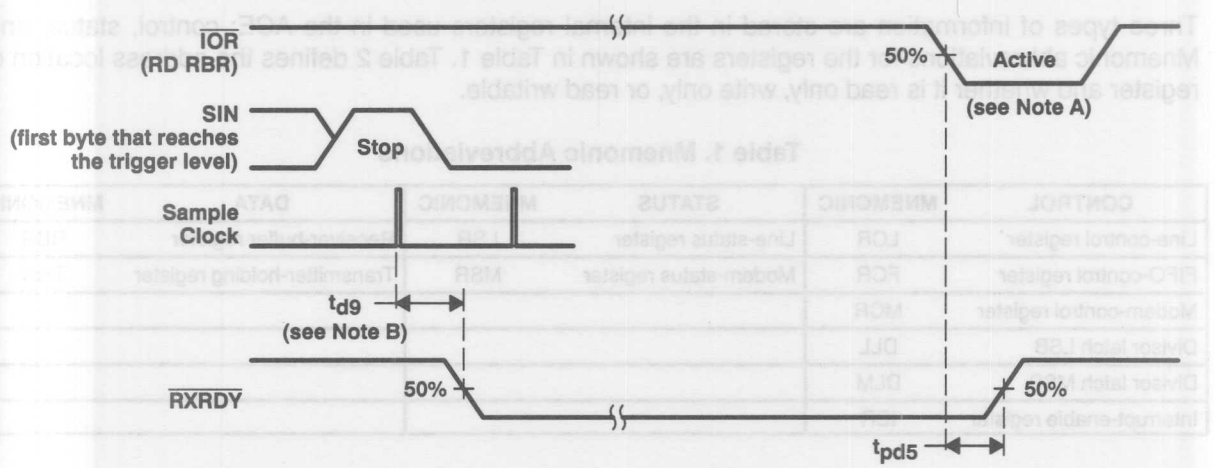
PARAMETER MEASUREMENT INFORMATION



NOTES: A. This is the reading of the last byte in the FIFO.
B. If FCR0 = 1, t_{d9} = 3 RCLK cycles. For a trigger-change-level interrupt, t_{d9} = 8 RCLK.

Figure 13. Receiver Ready-Mode 1 Timing Waveforms

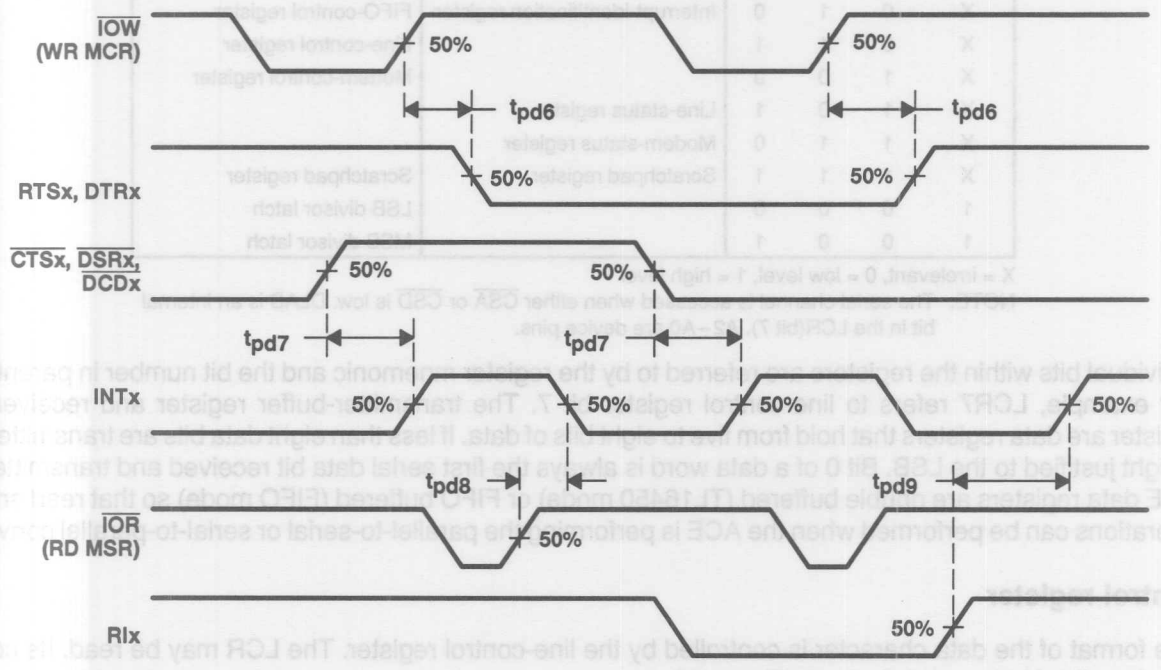


Figure 14. Modem Timing

PRINCIPLES OF OPERATION

Three types of information are stored in the internal registers used in the ACE: control, status, and data. Mnemonic abbreviations for the registers are shown in Table 1. Table 2 defines the address location of each register and whether it is read only, write only, or read writable.

Table 1. Mnemonic Abbreviations

CONTROL	MNEMONIC	STATUS	MNEMONIC	DATA	MNEMONIC
Line-control register	LCR	Line-status register	LSR	Receiver-buffer register	RBR
FIFO-control register	FCR	Modem-status register	MSR	Transmitter-holding register	THR
Modem-control register	MCR				
Divisor latch LSB	DLL				
Divisor latch MSB	DLM				
Interrupt-enable register	IER				

Table 2. Serial-Channel Internal Registers

DLAB	A2	A1	A0	READ MODE	WRITE MODE
0	0	0	0	Receiver-buffer register	Transmitter-holding register
0	0	0	1		Interrupt-enable register
X	0	1	0	Interrupt-identification register	FIFO-control register
X	0	1	1		Line-control register
X	1	0	0		Modem-control register
X	1	0	1	Line-status register	
X	1	1	0	Modem-status register	
X	1	1	1	Scratchpad register	Scratchpad register
1	0	0	0		LSB divisor latch
1	0	0	1		MSB divisor latch

X = irrelevant, 0 = low level, 1 = high level

NOTE: The serial channel is accessed when either $\overline{CSA}$ or $\overline{CSD}$ is low. DLAB is an internal bit in the LCR(bit 7). A2–A0 are device pins.

Individual bits within the registers are referred to by the register mnemonic and the bit number in parentheses. For example, LCR7 refers to line-control register bit 7. The transmitter-buffer register and receiver-buffer register are data registers that hold from five to eight bits of data. If less than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The ACE data registers are double buffered (TL16450 mode) or FIFO buffered (FIFO mode) so that read and write operations can be performed when the ACE is performing the parallel-to-serial or serial-to-parallel conversion.

line-control register

The format of the data character is controlled by the line-control register. The LCR may be read. Its contents are described below and shown in Figure 15.

LCR0 and LCR1, word-length select bits:

The number of bits in each serial character is programmed.

LCR2, stop-bit select bit:

LCR2 specifies the number of stop bits in each transmitted character. The receiver always checks for one stop bit.

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PRINCIPLES OF OPERATION

line-control register (continued)

LCR3, parity enable bit:

When LCR3 is high, a parity bit between the last data word bit and stop bit is generated and checked.

LCR4, even parity select bit:

When enabled, a logic one selects even parity.

LCR5, stick parity bit:

When parity is enabled (LCR3 = 1), LCR5 = 1 causes the transmission and reception of a parity bit to be in the opposite state from the value of LCR4. This forces parity to a known state and allows the receiver to check the parity bit in a known state.

LCR6, break-control bit:

When LCR6 is set to a logic 1, the serial outputs TXx are forced to the spacing state (low). The break-control bit acts only on the serial output and does not affect the transmitter logic. If the following sequence is used, no invalid characters are transmitted because of the break.

Step 1: Load a zero byte in response to the transmitter-holding-register empty (THRE) status indication.

Step 2: Set the break in response to the next THRE status indication.

Step 3: Wait for the transmitter to be idle when transmitter-empty status signal is set high (TEMT = 1); then clear the break when the normal transmission has to be restored.

LCR7, divisor-latch access bit (DLAB) bit:

Bit 7 must be set high (logic 1) to access the divisor latches DLL and DLM of the baud-rate generator during a read or write operation. LCR7 must be input low (logic 0) to access the receiver-buffer register, the transmitter-holding register, or the interrupt-enable register.

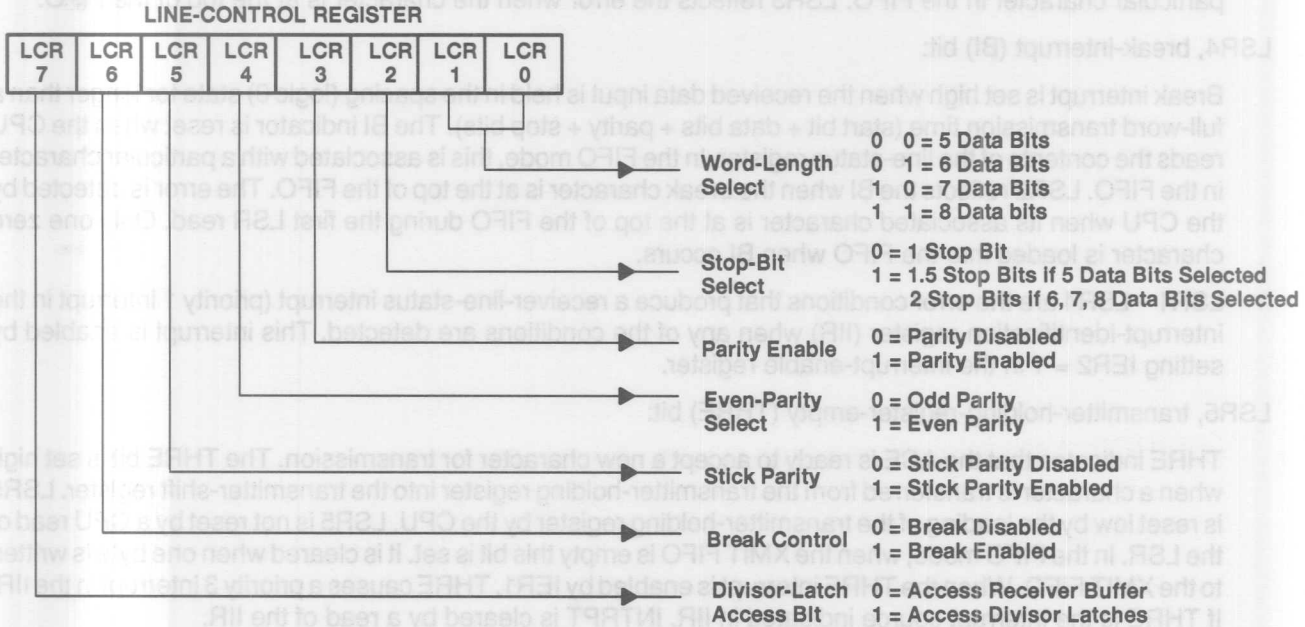

Figure 15. Line-Control Register Contents

PRINCIPLES OF OPERATION

line-status register

The line-status register (LSR) is a single register that provides status indications. The line-status register shown in Table 3 is described below:

LSR0, data-ready (DR) bit:

Data ready is set high when an incoming character is received and transferred into the receiver-buffer register or the FIFO. LSR0 is reset low by a CPU read of the data in the receiver-buffer register or the FIFO.

LSR1, overrun-error (OE) bit:

Overrun error indicates that data in the receiver-buffer register is not read by the CPU before the next character is transferred into the receiver buffer register overwriting the previous character. The OE indicator is reset whenever the CPU reads the contents of the line-status register. An overrun error occurs in the FIFO mode after the FIFO is full and the next character is completely received. The overrun error is detected by the CPU on the first LSR read after it happens. The character in the shift register is not transferred to the FIFO, but it is overwritten.

LSR2, parity-error (PE) bit:

Parity error indicates that the received data character does not have the correct parity as selected by LCR3 and LCR4. The PE bit is set high upon detection of a parity error and is reset low when the CPU reads the contents of the LSR. In the FIFO mode, the parity error is associated with a particular character in the FIFO. LSR2 reflects the error when the character is at the top of the FIFO.

LSR3, framing-error (FE) bit:

Framing error indicates that the received character does not have a valid stop bit. LSR3 is set high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset low when the CPU reads the contents of the LSR. In the FIFO mode, the framing error is associated with a particular character in the FIFO. LSR3 reflects the error when the character is at the top of the FIFO.

LSR4, break-interrupt (BI) bit:

Break interrupt is set high when the received data input is held in the spacing (logic 0) state for longer than a full-word transmission time (start bit + data bits + parity + stop bits). The BI indicator is reset when the CPU reads the contents of the line-status register. In the FIFO mode, this is associated with a particular character in the FIFO. LSR2 reflects the BI when the break character is at the top of the FIFO. The error is detected by the CPU when its associated character is at the top of the FIFO during the first LSR read. Only one zero character is loaded into the FIFO when BI occurs.

LSR1 – LSR4 are the error conditions that produce a receiver-line-status interrupt (priority 1 interrupt in the interrupt-identification register (IIR) when any of the conditions are detected. This interrupt is enabled by setting IER2 = 1 in the interrupt-enable register.

LSR5, transmitter-holding-register-empty (THRE) bit:

THRE indicates that the ACE is ready to accept a new character for transmission. The THRE bit is set high when a character is transferred from the transmitter-holding register into the transmitter-shift register. LSR5 is reset low by the loading of the transmitter-holding register by the CPU. LSR5 is not reset by a CPU read of the LSR. In the FIFO mode, when the XMIT FIFO is empty this bit is set. It is cleared when one byte is written to the XMIT FIFO. When the THRE interrupt is enabled by IER1, THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.

PRINCIPLES OF OPERATION

line-status register (continued)

LSR6, transmitter-register-empty (TEMT) bit:

TEMT is set high when the transmitter-holding register (THR) and the transmitter-shift register (TSR) are both empty. LSR6 is reset low when a character is loaded into THR and remains low until the character is transferred out of TXx. TEMT is not reset low by a CPU read of the LSR. In the FIFO mode, when both the transmitter FIFO and shift register are empty, this bit is set to one.

LSR7, RCVR-FIFO-error bit:

The LSR7 bit is always 0 in the TL16C450 mode (see FCR bit 0). In the FIFO mode, it is set when at least one of the following data errors is in the FIFO: parity error, framing error, or break-interrupt indication. It is cleared when the CPU reads the LSR if there are no subsequent errors in the FIFO.

NOTE: The line-status register may be written. However, this function is intended only for factory test. It should be considered as read only by applications software.

Table 3. Line-Status Register Bits

LSR BITS	1	0
LSR0 data ready (DR)	Ready	Not ready
LSR1 overrun error (OE)	Error	No error
LSR2 parity error (PE)	Error	No error
LSR3 framing error (FE)	Error	No error
LSR4 break interrupt (BI)	Break	No break
LSR5 transmitter-holding-register empty (THRE)	Empty	Not empty
LSR6 transmitter register empty (TEMT)	Empty	Not empty
LSR7 RCVR-FIFO error	Error in FIFO	No error in FIFO

FIFO-control register

The FIFO-control register is a write-only register at the same location as the IIR. It is used to enable the FIFOs, set the trigger level of the RCVR FIFO, and select the type of DMA signalling.

FCR0 enables both the XMIT and RCVR FIFOs. All bytes in both FIFOs can be cleared by resetting FCR0. Data is cleared automatically from the FIFOs when changing from the FIFO mode to the TL16C450 mode (see FCR bit 0) and vice versa. Programming of other FCR bits is enabled by setting FCR0 = 1.

FCR1 = 1 clears all bytes in the RCVR FIFO and resets its counter logic to 0. This does not clear the shift register.

FCR2 = 1 clears all bytes in the XMIT FIFO and resets the counter logic to 0. This does not clear the shift register.

FCR3 = 1 changes $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ from mode 0 to mode 1 if FCR0 = 1.

FCR4–FCR5: These two bits are reserved for future use.

FCR6–FCR7: These two bits are used for setting the trigger level for the RCVR FIFO interrupt as follows:

BIT		RCVR-FIFO TRIGGER LEVEL (BYTES)
7	6	
0	0	01
0	1	04
1	0	08
1	1	14

PRINCIPLES OF OPERATION

modem-control register

The modem-control register (MCR) controls the interface with the modem or data set as described in Figure 16. MCR can be written and read. The $\overline{RTS}$ and $\overline{DTR}$ outputs are directly controlled by their control bits in this register. A high input asserts a low (true) at the output pins. MCR bits 0, 1, 2, 3, and 4 are shown as follows:

MCR0: When MCR0 is set high, the $\overline{DTR}$ output is forced low. When MCR0 is reset low, the $\overline{DTR}$ output is forced high. The $\overline{DTR}$ output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR1: When MCR1 is set high, the $\overline{RTS}$ output is forced low. When MCR1 is reset low, the $\overline{RTS}$ output is forced high. The $\overline{RTS}$ output of the serial channel may be input into an inverting line driver to obtain the proper polarity input at the modem or data set.

MCR2: No effect on operation

MCR3: When MCR3 is set high, the external serial-channel interrupt is enabled.

MCR4: MCR4 provides a local loopback feature for diagnostic testing of the channel. When MCR4 is set high, serial output TXx is set to the marking (logic 1) state and the receiver data serial input (SIN) is disconnected. The output of the transmitter shift register is looped back into the receiver shift register input. The four modem-control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are disconnected. The modem-control outputs ($\overline{DTR}$ and $\overline{RTS}$) are internally connected to the four modem-control inputs. The modem-control output pins are forced to their inactive (high) state on the TL16C554. In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the selected serial channel. Interrupt control is fully operational; however, interrupts are generated by controlling the lower four MCR bits internally. Interrupts are not generated by activity on the external pins represented by those four bits.

MCR5 – MCR7: These three bits are permanently set to logic 0.

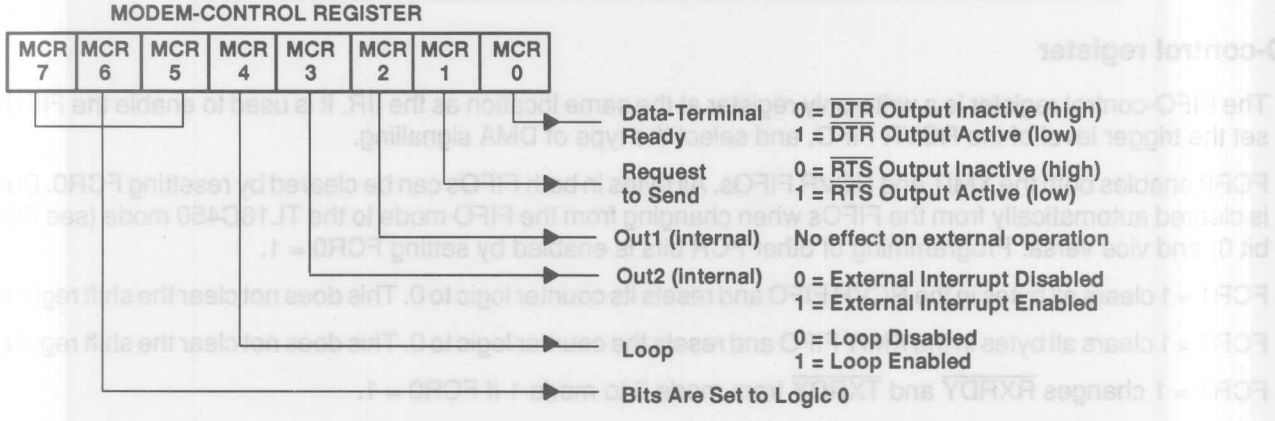

Figure 16. Modem-Control Register Contents

modem-status register

The modem-status register (MSR) provides the CPU with status of the modem input lines for the modem or peripheral devices. The MSR allows the CPU to read the serial-channel modem-signal inputs by accessing the data bus interface of the ACE in addition to the current status of four bits of the MSR that indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set high when a control input from the modem changes state and resets low when the CPU reads the MSR.

PRINCIPLES OF OPERATION

modem-status register (continued)

The modem input lines are $\overline{CTS}$, DSR, and $\overline{DCD}$. MSR4 – MSR7 are status indications of these lines. A status bit = 1 indicates the input is low. A status bit = 0 indicates the input is high. If the modem-status interrupt in the interrupt-enable register is enabled IIR3, an interrupt is generated whenever MSR0 – MSR3 is set to a one. The MSR is a priority 4 interrupt. The contents of the modem-status register are described in Table 4.

MSR0, delta-clear-to-send (ΔCTS) bit:

DCTS indicates that the $\overline{CTS}$ input to the serial channel has changed state since it was last read by the CPU.

MSR1, delta-data-set-ready (ΔDSR) bit:

ΔDSR indicates that the $\overline{DSR}$ input to the serial channel has changed state since the last time it was read by the CPU.

MSR2, trailing edge-of-ring-indicator (TERI) bit:

TERI indicates that the $\overline{RIx}$ input to the serial channel has changed state from low to high since the last time it was read by the CPU. High-to-low transitions on RI do not activate TERI.

MSR3, delta-data-carrier-detect (ΔDCD) bit:

ΔDCD indicates that the $\overline{DCD}$ input to the serial channel has changed state since the last time it was read by the CPU.

MSR4, clear-to-send (CTS) bit:

CTS is the complement of the $\overline{CTS}$ input from the modem indicating to the serial channel that the modem is ready to receive data from the serial channel's transmitter output (SOUT). If the serial channel is in the loop mode (MCR4 = 1), MSR4 reflects the value of RTS in the MCR.

MSR5, data-set-ready DSR bit:

DSR is the complement of the $\overline{DSR}$ input from the modem to the serial channel that indicates that the modem is ready to provide received data from the serial-channel receiver circuitry. If the channel is in the loop mode (MCR4 = 1), MSR5 reflects the value of DTR in the MCR.

MSR6, ring-indicator (RI) bit:

RI is the complement of the $\overline{RIx}$ inputs. If the channel is in the loop mode (MCR4 = 1), MSR6 reflects the value of $\overline{OUT1}$ in the MCR.

MSR7, data-carrier-detect (DCD) bit:

Data-carrier detect indicates the status of the data-carrier-detect ($\overline{DCD}$) input. If the channel is in the loop mode (MCR4 = 1), MSR7 reflects the value of OUT2 in the MCR.

Reading the MSR register clears the delta-modem status indications but has no effect on the other status bits. For LSR and MSR, the setting of status bits is inhibited during status-register read operations. If a status condition is generated during a read $\overline{IOR}$ operation, the status bit is not set until the trailing edge of the read. If a status bit is set during a read operation and the same status condition occurs, that status bit is cleared at the trailing edge of the read instead of being set again. In the loopback mode when modem-status interrupts are enabled, $\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$ and $\overline{DCD}$ inputs are ignored; however, a modem-status interrupt can still be generated by writing to MCR3–MCR0. Applications software should not write to the modem-status register.

PRINCIPLES OF OPERATION

modem-status register (continued)

Table 4. Modem-Status Register Bits

MSR BIT	MNEMONIC	DESCRIPTION
MSR0	ΔCTS	Delta clear to send
MSR1	ΔDSR	Delta data set ready
MSR2	TERI	Trailing edge of ring indicator
MSR3	ΔDCD	Delta data carrier detect
MSR4	CTS	Clear to send
MSR5	DSR	Data set ready
MSR6	RI	Ring indicator
MSR7	DCD	Data carrier detect

divisor latches

The ACE serial channel contains a programmable baud-rate generator (BRG) that divides the clock (dc to 8 MHz) by any divisor from 1 to $2^{16}-1$ (see also BRG description). Two 8-bit divisor-latch registers store the divisor in a 16-bit binary format. These divisor-latch registers must be loaded during initialization. Upon loading either of the divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load. The BRG can use any of three different popular frequencies to provide standard baud rates. These frequencies are 1.8432 MHz, 3.072 MHz, and 8 MHz. With these frequencies, standard bit rates from 50 kbps to 512 kbps are available. Tables 6, 7, 8, and 9 illustrate the divisors needed to obtain standard rates using these three frequencies. The output frequency of the baud generator is 16× the data rate [divisor # = clock + (baud rate × 16)] referred to in this document as RCLK.

scratchpad register

The scratchpad register is an 8-bit read/write register that has no effect on either channel in the ACE. It is intended to be used by the programmer to hold data temporarily.

interrupt-identification register

In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows:

1. Receiver-line status (priority 1)
2. Received-data ready (priority 2) or character time-out
3. Transmitter-holding-register empty (priority 3)
4. Modem status (priority 4)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the interrupt-identification register (IIR). The IIR indicates the highest priority interrupt pending. The contents of the IIR are indicated in Table 5.

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PRINCIPLES OF OPERATION

interrupt-identification register (continued)

Table 5. Interrupt-Control Functions

INTERRUPT-IDENTIFICATION REGISTER				INTERRUPT SET AND RESET FUNCTIONS			
BIT 3	BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT-RESET CONTROL
0	0	0	1	—	None	None	—
0	1	1	0	First	Receiver-line status	OE, PE, FE, or BI	LSR read
0	1	0	0	Second	Received data available	Receiver data available or trigger level reached	RBR read until FIFO drops below the trigger level
1	1	0	0	Second	Character time-out indication	No characters have been removed from or input to the receiver FIFO during the last four character times, and there is at least one character in it during this time.	RBR read
0	0	1	0	Third	THRE	THRE	IIR read if THRE is the interrupt source or THR write
0	0	0	0	Fourth	Modem status	$\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$, or $\overline{DCD}$	

IIR0 can be used to indicate whether an interrupt is pending. When IIR0 is low, an interrupt is pending.

IIR1 and IIR2 are used to identify the highest priority interrupt pending as indicated in Table 5.

IIR3: This bit is always logic 0 when in the TL16C450 mode. This bit is set along with bit 2 when in the FIFO mode and a trigger-change-level interrupt is pending.

IIR4 – IIR5: These two bits are always set to logic 0.

IIR6 – IIR7: FCR0 = 1 sets these two bits.

interrupt-enable register

The interrupt-enable register (IER) is used to independently enable the four serial-channel-interrupt sources that activate the interrupt (INTA, B, C, D) output. All interrupts are disabled by resetting IER0 – IER3 of the interrupt-enable register. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling the interrupt system inhibits the interrupt-identification register and the active (high) interrupt output. All other system functions operate in their normal manner, including the setting of the line-status and modem-status registers. The contents of the interrupt-enable register are shown in Table 10 described below:

IER0: When set to one, IER0 enables the received-data-available interrupt and the time-out interrupts in the FIFO mode.

IER1: When set to one, IER1 enables the transmitter-holding-register-empty interrupt.

IER2: When set to one IER2 enables the receiver-line-status interrupt.

IER3: When set to one, IER3 enables the modem-status interrupt.

IER4 – IER7: These four bits of the IER are logic 0.

PRINCIPLES OF OPERATION

receiver

Serial asynchronous data is input into the RXx terminal. The ACE continually searches for a high-to-low transition from the idle state. When the transition is detected, a counter is reset and counts the 16× clock to 7 1/2, which is the center of the start bit. The start bit is valid if the RXx is still low. Verifying the start bits prevents the receiver from assembling a false data character due to a low-going noise spike on the RXx input.

The line-control register determines the number of data bits in a character (LCR0, LCR1). If parity is used, LCR3 and the polarity of parity LCR4 are needed. Status for the receiver is provided in the line-status register. When a full character is received including parity and stop bits, the data-received indication in LSR0 is set high. The CPU reads the receiver-buffer register, which resets LSR0. If the character is not read prior to a new character transfer from the RSR to the RBR, the overrun-error-status indication is set in LSR1. If there is a parity error, the parity error is set in LSR2. If a stop bit is not detected, a framing-error indication is set in LSR3.

In the FIFO-mode operation, the data character and the associated error bits are stored in the receiver FIFO. If the data into RXx is a symmetrical square wave, the center of the data cells occurs within ±3.125% of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 16× clock cycle prior to being detected.

reset

After power up, the ACE RESET input should be held high for one microsecond to reset the ACE circuits to an idle mode until initialization. A high on RESET causes the following:

Initializes the transmitter and receiver internal clock counters

Clears the line-status register (LSR), except for transmitter-register empty (TEMT) and transmit-holding-register empty (THRE), which are set. The modem-control register (MCR) is also cleared. All of the discrete lines, memory elements, and miscellaneous logic associated with these register bits are also cleared or turned off. The line-control register (LCR), divisor latches, receiver-buffer register, and transmitter-buffer register are not affected.

Following the removal of the reset condition (RESET low), the ACE remains in the idle mode until programmed. A hardware reset of the ACE sets the THRE and TEMT status bits in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE. A summary of the effect of a reset on the ACE is given in Table 10.

programming

The serial channel of the ACE is programmed by the control registers LCR, IER, DLL, DLM, MCR, and FCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface.

While the control registers can be written in any order, the IER should be written last because it controls the interrupt enables. Once the serial channel is programmed and operational, these registers can be updated any time the ACE serial channel is not transmitting or receiving data.

PRINCIPLES OF OPERATION

FIFO-interrupt-mode operation

The following RCVR status occurs when the RCVR FIFO and receiver interrupts are enabled.

1. LSR0 is set when a character is transferred from the shift register to the RCVR FIFO. When the FIFO is empty, it is reset.
2. IIR = 06 receiver-line-status interrupt has higher priority than the receive-data-available interrupt IIR = 04.
3. Receive-data-available interrupt is issued to the CPU when the programmed trigger level is reached by the FIFO. As soon as the FIFO drops below its programmed trigger level, it is cleared.
4. IRR = 04 (receive-data-available indication) also occurs when the FIFO reaches its trigger level. It is cleared when the FIFO drops below the programmed trigger level.

The following RCVR FIFO character time-out status occurs when RCVR FIFO and receiver interrupts are enabled.

1. If the following conditions exist, a FIFO character time-out interrupt occurs:
   - Minimum of one character in FIFO
   - Last received serial character is longer than four continuous previous character times ago. (If two stop bits are programmed, the second one is included in the time delay.)
   - The last CPU read of the FIFO is more than four continuous character times earlier. At 300 baud and 12-bit characters, the FIFO time-out interrupt causes a latency of 160 ms maximum from received character to interrupt issued.
2. By using the XTAL1 input for a clock signal, the character times can be calculated. The delay is proportional to the baud rate.
3. The time-out timer is reset after the CPU reads the RCVR FIFO or after a new character is received. This occurs when there has been no time-out interrupt.
4. A time-out interrupt is cleared and the timer is reset when the CPU reads a character from the RCVR FIFO.

XMIT interrupts occurs as follows when the transmitter and XMIT FIFO interrupts are enabled (FCR0 = 1, IER = 1).

1. When the transmitter FIFO is empty, the transmitter-holding-register interrupt (IIR = 02) occurs. The interrupt is cleared when the transmitter-holding register is written to or the IIR is read. One to sixteen characters can be written to the transmit FIFO when servicing this interrupt.
2. The transmitter FIFO empty indications are delayed one character time minus the last-stop bit time whenever the following occurs:

   THRE = 1, and there has not been a minimum of two bytes at the same time in XMIT FIFO since the last THRE = 1. The first transmitter interrupt after changing FCR0 is immediate, however, assuming it is enabled.

RCVR-FIFO-trigger level and character time-out interrupts have the same priority as the receive-data-available interrupt. The transmitter-holding-register-empty interrupt has the same priority as the transmitter-FIFO-empty interrupt.

PRINCIPLES OF OPERATION

FIFO-polled-mode operation

Resetting IER0, IER1, IER2, IER3, or all to zero with FCR0 = 1 puts the ACE into the FIFO-polled mode. RCVR and XMITER are controlled separately. Either or both can be in the polled mode.

In the FIFO-polled mode, there is no time-out condition indicated or trigger level reached. However, the RCVR and XMIT FIFOs still have the capability of holding characters. The LSR must be read to determine the ACE status.

$\overline{\text{TXRDY}}$ operation

In mode 0, $\overline{\text{TXRDY}}$ is asserted (low) when the transmit FIFO is empty; it is released (high) when the FIFO contains at least one byte. In this way, the FIFO is written with 16 bytes when $\overline{\text{TXRDY}}$ is asserted (low).

In mode 1, $\overline{\text{TXRDY}}$ is asserted (low) when the transmit FIFO is not full; in this mode, the transmit FIFO is written with another byte when $\overline{\text{TXRDY}}$ is asserted (low).

$\overline{\text{RXRDY}}$ operation

In mode 0, $\overline{\text{RXRDY}}$ is asserted (low) when the receive FIFO is not empty; it is released (high) when the FIFO is empty. In this way, the receive FIFO is read when $\overline{\text{RXRDY}}$ is asserted (low).

In mode 1, $\overline{\text{RXRDY}}$ is asserted (low) when the receive FIFO has filled to the trigger level or a character time-out has occurred (four character times with no transmission of characters); it is released (high) when the FIFO is empty. In this mode, multiple received characters are read by the DMA device, reducing the number of times it is interrupted.

$\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ outputs from each of the four internal ACEs of the TL16C554 are ANDed together internally. This combined signal is brought out externally to $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$.

PRINCIPLES OF OPERATION

Table 6. Baud Rates (1.8432-MHz Clock)

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	—
75	1536	—
110	1047	0.026
134.5	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.690
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.860

Table 7. Baud Rates (3.072-MHz Clock)

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	—
75	2560	—
110	1745	0.026
134.5	1428	0.034
150	1280	—
300	640	—
600	320	—
1200	160	—
1800	107	0.312
2000	96	—
2400	80	—
3600	53	0.628
4800	40	—
7200	27	1.230
9600	20	—
19200	10	—
38400	5	—

PRINCIPLES OF OPERATION

Table 8. Baud Rates (8-MHz Clock)

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	10000	—
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	333	0.010
300	1667	0.020
600	883	0.040
1200	417	0.080
1800	277	0.080
2000	250	—
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344
512000	1	2.400

PRINCIPLES OF OPERATION

Table 9. Baud Rates (16-MHz Clock)

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	20000	0
75	13334	0.00
110	9090	0.01
134.5	7434	0.01
150	6666	0.01
300	3334	−0.02
600	1666	0.04
1200	834	−0.08
1800	554	0.28
2000	500	0.00
2400	416	0.16
3600	278	−0.08
4800	208	0.16
7200	138	0.64
9600	104	0.16
19200	52	0.16
38400	26	0.16
56000	18	−0.79
128000	8	−2.34
256000	4	−2.34
512000	2	−2.34
1000000	1	0.00

Table 10. Reset

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt-enable register	Reset	All bits low (0–3 forced and 4–7 permanent)
Interrupt-identification register	Reset	Bit 0 is high, bits 1, 2, 3, 6, and 7 are low, Bits 4–5 are permanently low
Line-control register	Reset	All bits low
Modem-control register	Reset	All bits low (5–7 permanent)
FIFO-control register	Reset	All bits low
Line-status register	Reset	All bits low, except bits 5 and 6 are high
Modem-status register	Reset	Bits 0–3 low, bits 4–7 input signals
TXx	Reset	High
Interrupt (RCVR errs)	Read LSR/Reset	Low
Interrupt (RCVR data ready)	Read RBR/Reset	Low
Interrupt (THRE)	Read IIR/Write THR/Reset	Low
Interrupt (modem status changes)	Read MSR/Reset	Low
$\overline{RTS}$	Reset	High
$\overline{DTR}$	Reset	High

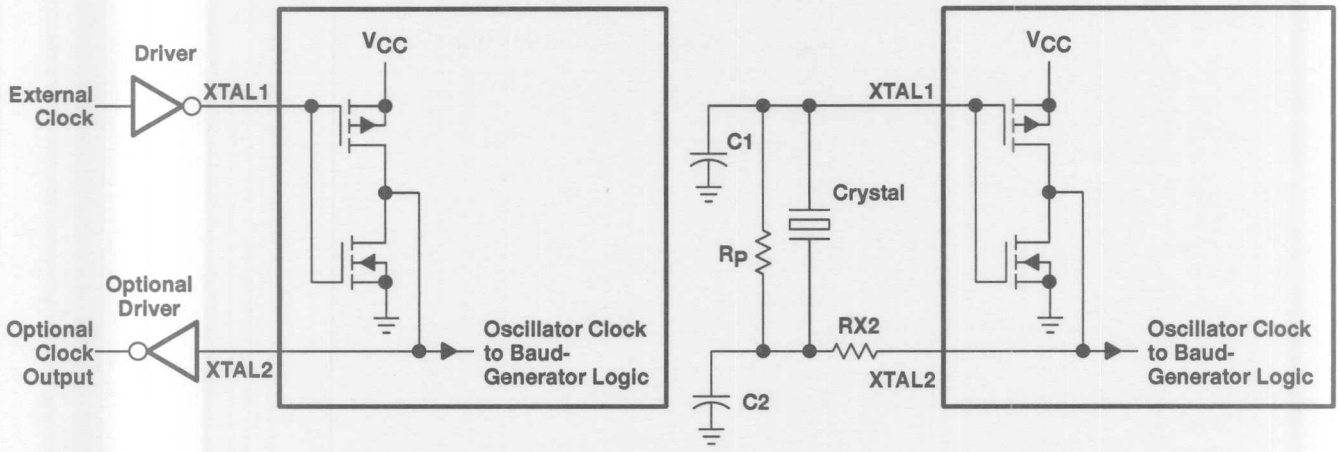
PRINCIPLES OF OPERATION

Table 11. Serial-Channel Accessible Registers

ADDRESS	REGISTER MNEMONIC	REGISTER ADDRESS							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	RBR (read only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)
0	THR (write only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
0†	DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1†	DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
1	IER	0	0	0	0	(EDSSI) Enable-modem-status interrupt	(ERLSI) Enable-receiver-line-status interrupt	(ETBEI) Enable-transmitter-holding-register-empty interrupt	(ERBI) Enable-received-data-available interrupt
2	FCR (write only)	RCVR Trigger (MSB)	RCVR Trigger (LSB)	Reserved	Reserved	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO Enable
2	IIR (read only)	FIFOs Enabled‡	FIFOs Enabled‡	0	0	Interrupt ID Bit (3)‡	Interrupt ID Bit (2)	Interrupt ID Bit (1)	0 If interrupt pending
3	LCR	(DLAB) Divisor-latch access bit	Set break	Stick parity	(EPS) Even-parity select	(PEN) Parity enable	(STB) Number of stop bits	(WLSB1) Word-length select bit 1	(WLSB0) Word-length select bit 0
4	MCR	0	0	0	Loop	OUT2 Enable external interrupt (INT)	Reserved	(RTS) Request to send	(DTR) Data terminal ready
5	LSR	Error in RCVR FIFO‡	(TEMT) Transmitter-registers empty	(THRE) Transmitter-holding-register empty	(BI) Break interrupt	(FE) Framing error	(PE) Parity error	(OE) Overrun error	(DR) Data ready
6	MSR	(DCD) Data-carrier detect	(RI) Ring indicator	(DSR) Data-set ready	(CTS) Clear to send	(ΔDCD) Delta-data-carrier detect	(TERI) Trailing-edge ring indicator	(ΔDSR) Delta-data-set ready	(ΔCTS) Delta-clear to send
7	SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

† DLAB = 1
‡ These bits are always 0 when FIFOs are disabled.

PRINCIPLES OF OPERATION



TYPICAL CRYSTAL OSCILLATOR NETWORK

CRYSTAL	Rp	RX2	C1	C2
3.1 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF
1.8 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF

Figure 17. Typical Clock Circuits

NOTES